DIGITAL SIGNAL PROCESSING APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a digital signal processing apparatus and, more particularly, to a digital signal processing apparatus for suppressing aliasing noise which is caused in association with half-band processing of a digital filter.

2. Description of the Background Art

In accordance with the advancement of digital technologies, various digital signal processing technologies are proposed in wide fields. In the above-mentioned digital signal processing, an analog input signal is converted into a digital signal by an analog/digital (hereinafter, referred to as an A/D) converter and then is subjected to various signal processing by latter-stage circuits. A digital filter serving as a general digital signal processing circuit performs calculation for a plurality of sampling data which is continuously inputted, attenuates a frequency component other than a normal band from among frequency components included in sampling outputs, and extracts only desired frequency component data. In general, the digital filter uses a method for increasing the number of sampling data so as to improve an S/N ratio. However, the increase in the number of sampling data causes the increase in circuit scale and the increase in number of calculation times, and the prolongation of calculation time.

Generally, half-band processing is well-known to solve the problem. In the half-band processing, an effect to reduce the number of elements is increased as the number of sampling data is larger, and the calculation processing is facilitated by using the principle in that the S/N ratio of an output value is not changed upon setting a coefficient, which is multiplied by even-th sampling data, to be zero when the number of sampling data serving as a first processing target is odd. Since the coefficient is zero, the number of calculation times is half. As a consequence, the numbers of multiplies, adders, and complement control circuits and a bit length of each register can be reduced.

However, since processing for the even-th sampling data is not performed in the half-band processing of the above-mentioned digital filter, it is equivalent that a sampling rate is reduced to be 1/2. Then, aliasing-noise pass band upon reducing the sampling rate is caused.

FIG. 1 is a diagram showing pass band characteristics of an output signal from the digital filter, in which the aliasing-noise is caused by the half-band processing, according to a background art. An aliasing band 1 occurred by the half-band processing is caused near a half frequency of a sampling frequency of the digital filter, as a pass band different from a normal band 2 serving as an original pass band. Therefore, the analog input signal includes a frequency component having the above band and, when the frequency component has an influence on signal processing

at the latter stage of the digital filter, the half-band processing cannot be used. Even in the case of purposely using the half-band processing, a digital low-pass filter for anti-aliasing is necessary at the latter stage of the digital filter. However, the digital low-pass filter needs calculation processing for a digital filter output and, therefore, the circuit scale and the number of calculation times are increased and the calculation time is long. An advantage for using the half-band processing to the digital filter is lost.

SUMMARY OF THE INVENTION

The present invention is devised in consideration of the above circumstances and it is an object of the present invention to provide a digital signal processing apparatus capable of suppressing or reducing aliasing noise which is caused in the half-band processing, with a simple circuit and reduced costs.

To accomplish the above object, according to a first aspect of the present invention, there is provided a digital signal processing apparatus, comprising: 1. A digital signal processing apparatus comprising: an A/D converter for converting an analog input signal into a digital signal; a digital filter for performing half-band processing to a sampling output of a digital signal outputted by the A/D converter and for attenuating a frequency component other than a predetermined normal band

from a frequency component included in the sampling output; and an anti-aliasing circuit for suppressing or removing noise having an aliasing band, which is caused by the half-band processing in the digital filter, by using a sign signal outputted from the digital filter. Accordingly, a simple circuit structure can suppress the aliasing noise with low costs.

Advantageously, the anti-aliasing circuit may determine whether the output from the digital filter, which is subjected to the half-band processing, is a pass signal having the normal band or a pass signal having the aliasing signal, based on a changing period of the sign signal outputted from the digital filter, and may suppress or remove only the pass signal having the aliasing band. With the above anti-aliasing circuit, since only the aliasing noise can be attenuated, a low-pass filter which has conventionally been needed is not arranged at the latter stage of the digital filter.

Advantageously, the anti-aliasing circuit may comprise: a period measuring circuit for measuring a changing period of the sign signal outputted by the digital filter; a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band; a comparator for comparing and determining whether or not the period measured by the period measuring circuit is larger than the threshold which is set to the threshold holding circuit and for outputting a shift

control signal when it is determined that the period measured by the period measuring circuit is not larger than the threshold; and a shift register for shifting a signal which is inputted from the digital filter and is stored, based on the shift control signal, and for suppressing an amplitude of the aliasing noise. Accordingly, the attenuation of the aliasing noise can be controlled with high accuracy.

Advantageously, the anti-aliasing circuit may further comprise a shift value setting register, to which the number of shift bits is set when the signal, which is inputted from the digital filter and is stored, is subjected to shift processing by the shift register. Accordingly, the attenuation amount of the output data from the digital filter can arbitrarily be adjusted when the aliasing noise is detected.

Advantageously, the anti-aliasing circuit may further comprise a delay circuit for delaying the output from the digital filter by a delay time which is taken by the measurement by the period measuring circuit and the comparison calculation by the comparator. Accordingly, the shit operation of the shift register, to which the delay data at the same time based on the output of the comparator, can be embodied with high accuracy.

Advantageously, the anti-aliasing circuit may comprise: a period measuring circuit for measuring a changing period of the sign signal which is outputted by

the digital filter; a threshold holding circuit for holding a period of an intermediate frequency between the normal band and the aliasing band; a comparator for comparing and determining whether or not the period measured by the period measuring circuit is larger than the threshold set to the threshold holding circuit and for outputting a clear signal when it is determined that the period is not larger than the threshold; and a delay circuit for delaying the output from the digital filter by a delay time which is taken by the measurement of the period measuring circuit and the comparison calculation of the comparator and for erasing a signal during delay processing when the clear signal is inputted. Accordingly, the output of the unnecessary aliasing noise component can be prevented with the simple structure.

According to a second aspect of the present invention, there is provided a digital signal processing apparatus comprising: an A/D converter for converting an analog input signal into a digital signal; a digital filter for performing half-band processing to a sampling output of a digital signal outputted by the A/D converter and for attenuating a frequency component other than a predetermined normal band from a frequency component included in the sampling output; an edge-detection circuit for detecting an edge of a sign signal which is outputted by the digital filter and for generating a set pulse; a period measuring circuit for measuring a changing period of

the sign signal which is outputted by the digital filter; a threshold holding circuit for holding a period of an intermediate frequency between a normal band and an aliasing band; a comparator for comparing and determining whether or not the period measured by the period measuring circuit is larger than the threshold held by the threshold holding circuit and for outputting a reset pulse when it is determined that the period is not larger than the threshold; and a detection register for inputting the set pulse so as to be in a set state and outputting a first level and for inputting the reset pulse so as to be in the reset state and outputting a second level. Accordingly, erroneous detection upon passage of the aliasing noise can be prevented.

The above and other objects and features of the present invention will become apparent from the following detailed description and the appended claims with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagram showing pass band characteristics of an output signal of a digital filter, in which aliasing noise is caused by a half-band processing of a digital filter, according to a background art of the present invention;

FIG. 2 is a block diagram showing a digital signal processing apparatus according to a first embodiment of the

present invention;

FIG. 3 is a block diagram specifically showing one example of an anti-aliasing circuit shown in FIG. 2 according to the first embodiment of the present invention;

FIG. 4 is a flowchart showing a processing routine of digital signal processing of the present invention;

FIG. 5 is a timing chart of signals of block units in FIG. 3;

FIG. 6 is a block diagram specifically showing another example of the anti-aliasing circuit according to the first embodiment of the present invention;

FIG. 7 is a block diagram specifically showing further another example of the anti-aliasing circuit according to the first embodiment of the present invention;

FIG. 8 is a block diagram showing a detection device using a sign output of the digital filter according to a second embodiment of the present invention; and

FIG. 9 is a timing chart of signals of block units in FIG. 8.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a preferred embodiment of the present invention will be described in detail with reference to the drawings. Then, the embodiment of the present invention is shown as follows and, however, the present invention is not limited to the following.

FIG. 2 is a block diagram showing a digital signal

processing apparatus according to a second embodiment of the present invention. Referring to FIG. 2, the digital signal processing apparatus comprises: an A/D converter 3 for converting an analog input signal 10 into a digital signal; a digital filter 4; and an anti-aliasing circuit 6 provided at the latter stage of the digital filter 4, for suppressing aliasing noise by using a sign signal 5 outputted from the digital filter 4. The anti-aliasing circuit 6 determines whether the signal from the digital filter 4 is a signal having a normal band or the aliasing noise, by using a changing period of the sign signal 5, and attenuates only an aliasing noise component of the output from the digital filter 4. Consequently, although the half-band processing has not been used for the digital filter under the limitation of the number of mounted elements, it can be used for the digital filter. The digital filter purposely using the half-band processing does not need the low-pass filter which is arranged at the latter stage of the digital filter. For example, when both the sampling data and the coefficient are 10 bits, several thousands of elements are necessary for each multiplier. On the other hand, the anti-aliasing circuit 6 comprises approximately one thousand elements. Therefore, an effect in that several thousands to several tens thousands elements can be reduced can be obtained without using the low-pass filter.

FIG. 3 is a block diagram specifically showing one

example of the anti-aliasing circuit in the digital signal processing apparatus. The digital signal processing apparatus comprises the A/D converter 3, the digital filter 4, and the anti-aliasing circuit 6. An analog input signal 10 is converted into a digital data signal D1 by the A/D converter 3. A frequency component within a preventing area, included in the digital data signal D1, is attenuated by the digital filter 4 which is subjected to the half-band processing. However, the aliasing noise, which is caused by the half-band processing, is mixed in an output signal D2 from the digital filter 4. The output signal D2 of the digital filter 4 is inputted to the anti-aliasing circuit 6.

The anti-aliasing circuit 6 comprises: a period measuring circuit 14; a threshold holding circuit 11; a comparator 12, a shift register 13, and a delay circuit 15. The period measuring circuit 14 measures a changing period of a sign signal 5 which is outputted by the digital filter 4. The threshold holding circuit 11 holds a threshold for a sign changing period. The comparator 12 determines whether the period measured by the period measuring circuit 14 is larger than the threshold held in the threshold holding circuit 11. If it is determined that the period is not larger than the threshold, the comparator 12 outputs a shift control signal 16. When the shift control signal 16 is at an active level, the shift register 13 shifts a signal D3 inputted from the digital filter 4 and stored, thereby suppressing amplitude of the aliasing noise. The

delay circuit 15 delays the output from the digital filter 4 by a delay time which is taken by the measurement of the period measuring circuit 14 and the comparison calculation of the comparator 12.

As shown in FIG. 1, a normal-band signal of the digital filter 4 becomes low in an output frequency band of the digital filter 4, and the aliasing noise becomes approximately half of the sampling frequency of the digital filter 4. A signal having an intermediate frequency band between the normal-band signal and the aliasing noise is attenuated by the original function of the digital filter 4. Therefore, the sign changing period of the signal which passes through the normal band, is clearly different from the sign changing period of the noise signal which passes through the aliasing band.

The comparator 12 can clearly determine whether the signal from the digital filter 4 is the normal-band signal or the aliasing noise, by setting the sign changing period of the intermediate frequency between the normal band and the aliasing band, to the threshold holding circuit 11. If the period measured by the period measuring circuit 14 is longer than the sign changing period set to the threshold holding circuit 11, the comparator 12 sets the shift control signal 16 to be "0" as the normal-band signal. If it is shorter than, the comparator 12 sets the shift control signal 16 to be "1" as the active level and as the aliasing noise. The shift control signal 16 from the

comparator 12 is used as the shift control signal 16 of the shift register 13. If the shift control signal 16 is "0", the shift operation is not performed. If it is "1", the shift operation is performed by one bit in an LSB (least significant bit) direction. Consequently, the amplitude of only the aliasing noise can be attenuated to be half. In the above processing, it is determined whether or not the shift operation is performed at the sign changing point and no glitch is therefore caused without discontinuous change of a phase of an output signal 17.

A next operation will be described with reference to a flowchart shown in FIG. 4 and a timing chart shown in FIG. 5. First, if the analog input signal 10 is inputted (step S1), the A/D converter 3 converts the analog input signal 10 into the digital data signal D1 (step S2). The sampling data of the digital data signal D1 is inputted to the digital filter 4 and is subjected to the half-band processing (step S3). The output subjected to the half-band processing is delayed by the delay circuit 15 (step S4). Further, the delay signal is under the shift control by the shift register 13 (step S5), and is sequentially outputted (step S6).

Referring to FIG. 5, a waveform 18 represents an analog input signal 10 and a waveform 19 represents an amplitude image of the output signal D2 of the digital filter 4, which is subjected to the half-band processing. Intervals 20 and 21 in the waveform 19 represent the

normal-band signal. As shown by an interval 22, the aliasing noise to be inherently attenuated passes through the digital filter 4 because it is subjected to the half-band processing. A waveform 23 represents the sign change of the waveform 19. As shown by the waveform 23, a period difference between a sign changing period N of the normal-band signal and a sign changing period M of the aliasing noise signal, clearly exists through the digital filtering processing.

Referring back to FIG. 4, the sign changing period of the sign signal 5 is measured based on the output signal D2 after the half-band processing (step S7). The measured sign changing period of the sign signal 5 is compared with a threshold A (step S8). The threshold A is set in advance to establish a relationship of (sign changing period M < threshold A < sign changing period N). If the comparison result, when the sign changing period M is smaller than the threshold A, is "1", the shift control signal 16 serving as the comparison result becomes "1" only during the occurrence of the aliasing noise, as shown by a waveform 24. Therefore, the shift control signal 16 can be used as a detection signal of the aliasing band pass signal. Incidentally, the waveform 24 is delayed from the waveform 19 by a delay time Td. Thus, the output signal D2 of the digital filter 4 shown by the waveform 19 is subjected to the delay processing by the delay time Td by the delay circuit 15. Then, the output signal D2 is stored in the

shift register 13 as the signal D3 shown by an amplitude image waveform 25. The signal shown by the waveform 24 is obtained as the comparison result and is inputted to the shift register 13 as the shift control signal 16.

If the sign changing period M is smaller than the threshold A, that is, if the waveform 24 is "1", the shift register 13 assumes that the aliasing noise is inputted and then shifts the output from the digital filter 4 at the same time, which is stored in the shift register 13, in the LSB direction by one bit (step S9), and suppresses the amplitude to be half. On the other hand, if the sign changing period is larger than the threshold A, that is, if the waveform 24 is "0", the shift register 13 assumes that the normal-band signal is inputted and a signal indicating that the shift operation is not performed is outputted (step S10). The signal is outputted without the shift processing of the shift register 13 (steps S5 and S6). In this case, a waveform 26 represents an amplitude image of an output signal 17 of the shift register 13. As described above, the amplitude of only the aliasing noise can be suppressed without changing the amplitude of the normal-band signal.

FIG. 6 is a diagram showing another example of the anti-aliasing circuit according to the first embodiment of the present invention. In the anti-aliasing circuit shown in FIG. 6, a shift value setting register 27 for controlling the number of bits of the shift register 13 is

newly added. Consequently, the amount of attenuation of the output data from the digital filter 4 can arbitrarily be adjusted when the aliasing noise is detected. Namely, when a number n of bits of the shift register 13 is set to the shift value setting register 27, an amplitude of the output data is 1/(2n).

FIG. 7 is a diagram showing further another example of the anti-aliasing circuit according to the first embodiment of the present invention. Herein, the shift register 13 shown in Fig. 2 is deleted and the output of the comparator 12 is set to be a clear signal 29 of the delay circuit 28. The delay circuit 28 delays the output from the digital filter 4 by a delay time which is taken by the measurement of the period measuring circuit 14 and by the comparison calculation of the comparator 12, and erases a signal during the delay processing when the clear signal 29 is inputted. With the above-mentioned structure, the unnecessary aliasing noise component can completely be removed.

FIG. 8 is a block diagram of a detection device using a sign signal of the output from the digital filter according to a second embodiment of the present invention, and FIG. 9 is a timing chart of signals from block units in FIG. 8. In a detection device 7 shown in FIG. 8, the period measuring circuit 14 measures a sign changing period of a sign signal 34 from the digital filter 4, and the comparator 12 compares the measured sign changing period

with the threshold which is set to the threshold holding circuit 11. If the sign changing period measured by the period measuring circuit 14 is smaller than the threshold, it is determined that the aliasing noise is detected and a reset pulse 35 is generated. A waveform 39 shown in FIG. 9 represents an amplitude image of an output 33 from the digital filter 4. The sign signal 34 from digital filter 4 is inputted to an edge-detection circuit 30, a rise edge is detected, and a set pulse 36 is generated to a detection register 31. By adding the reset pulse 35 to a reset terminal of the detection register 31, an output signal 38 of the detection register 31 is set to be "0" during detection of the aliasing noise and erroneous detection due to the aliasing noise is prevented. Incidentally, if the set pulse 36 is not inputted to the detection register 31 during a period $(T + \Delta T)$ which is longer than a sign changing period T of the output 33 from the digital filter 4, a state-detection circuit 32 outputs the reset pulse 35 to the detection register 31.

As mentioned above, in the present invention, since the aliasing noise caused by the half-band processing is suppressed or removed by using the sign signal of the output from the digital filter for the half-band processing, the half-band processing can be used for the digital filter though it has not been used for the digital filter due to the effect of the aliasing noise. The anti-aliasing method can be embodied with low costs because the aliasing noise

caused by the half-band processing is suppressed or removed by using the shift register and the simple control circuit instead of the low-pass filter. In particular, as the digital filter needs a higher S/N ratio, advantageously, costs can be reduced because input sampling data and bit length of the coefficient to which the input sampling data is multiplied, are prolonged.